METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE HAVING THIN FILM SOI STRUCTURE

CROSS-REFERENCE TO RELATED APPLICATION

This application claims the priority benefit of Japanese Patent Application No. 2001-384956, filed December 18, 2001, the entire disclosure of which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the invention

The invention relates to a method of manufacturing a semiconductor device, specifically to a method of manufacturing a semiconductor device having a thin film SOI structure in which imperceptible contact holes are formed.

2. Description of the related art

With an increase in the level of a high performance, an SOI-type semiconductor device is generally used in order to satisfying the requirement, instead of a semiconductor device having a bulk silicon substrate. The SOI-type semiconductor device includes an SOI substrate, which consists of a support substrate, a buried silicon oxide layer (BOX layer) and a silicon layer (SOI layer) formed on the BOX layer, and field effect transistors (FETs) are formed in the silicon layer. Thus, this type of the semiconductor device is called SOI (Silicon On Insulator) type semiconductor

device.

According to the SOI-type semiconductor device, since the FETs are formed in a thin SOI layer formed on a BOX layer, a junction capacitance can be reduced, comparing to the semiconductor device having the bulk silicon substrate. As a result, high speed performance can be expected in such a SOI-type semiconductor device. Further, it is easy to isolate electrically each FET because the FETs are formed on the thin SOI layer. Specifically, the FETs are formed on the thin SOI layer, these FETs become fully depleted FETs. Thus, each fully depleted FET has small parasitic capacitance so that sub-threshold swing in the SOI-type semiconductor device becomes smaller than that in the semiconductor device having the bulk silicon substrate. As a result, the SOI-type semiconductor device draws attention as a low power consumption device. Moreover, since the width of the depletion region of each FET at its channel is determined by the thickness of the thin SOI layer, it is possible to control the short channel effect.

To perform the fully depleted operation of the SOI-type semiconductor device, it is required that the thickness of the SOI layer be reduced, with the progress of development of imperceptible device. For example, as shown in a thesis "Deep Sub-0.1μm MOSFET's with very thin SOI layer for ultra-low power consumption", C-II vol. J81-C-II No. 3, pp 313-319 published in 1998 by The Institute of Electronics, Information and Communication Engineers, the shorter the gate length is, like 0.35μm, 0.25 μm, and 0.18 μm, the thinner the thickness of the SOI layer is, like 60nm, 50nm,

and 40nm. In the generation that the gate length is 0.1 μm, it is required that the thickness of the SOI layer be less than 20nm.

When the thickness of the SOI layer becomes thinner, an operation ability using current may be decreased because the parasitic resistance at diffusion layers such as source and drain layers, increases. To avoid this issue, a silicide layer, such as a $TiSi_x$ layer or a $CoSi_x$ layer, is formed on the source and drain, whereby it is possible to reduce the resistance value. If the $CoSi_x$ layer is selected, three possible formations can be considered: one is Co_2Si, another is CoSi, and the other is $CoSi_2$. Since $CoSi_2$ has the lowest resistance value among them, the $CoSi_2$ layer may be selected and is selectively formed on the SOI substrate by the following process.

First, a Co layer is formed on the thin SOI layer. Then, a first anneal treatment is performed in the atmosphere of 550 ℃ for 30 seconds, and a second anneal treatment is performed in the atmosphere of 700 ℃ for 60 seconds successively. By performing the first and the second anneal treatments under the condition described above, the $CoSi_2$ layer can be formed consistently. The process of forming a $CoSi_2$ layer are reported in "Optimization of Series Resistance in Sub-0.2 mm SOI MOSFET's", IEEE Electron device letters, Vol. 15, No. 09 Page 363 published in 1994.

However, the thinner the SOI layer is, the lesser the amount of silicon in the SOI layer to be consumed is. As a result, when the silicide layer is formed with using the thin SOI layer, it is difficult to control the composition in order to form the silicide layer consistently. Further, since the thickness of the SOI layer is reduced gradually

by factors presented in each of the process steps before silicidation, it is further difficult to control the composition in order to form the silicide layer. As a result of this difficulty, a localized thin regions or defect spots of silicided SOI (void) may be formed during the $CoSi_2$ silicidation process at the second anneal treatment. Specifically, since it is generally found that the SOI layer is thinner in some areas (it is called "local thinning"), there is strong possibility that voids are preferentially formed in this areas during silicidation of the SOI layer. In the successive process for forming a contact hole in an insulating layer, which is formed on the silicide layer, when the contact holes are formed at the areas where the voids are formed, the contact holes reach the BOX layer underneath the silicide layer via voids. Since the BOX layer is formed of the same material (SiO2) of the insulating layer, the contact hole may reaches to the support substrate easily in case of the over-etching, resulting in the formation of threading pinholes through the BOX layer at the contact opening. In other words, the BOX layer can not stop etching for forming the contact hole because the insulating layer and the BOX layer are formed of the same material. As a result, a process yield (hereinafter referred as a BOX yield) is dramatically decreased.

SUMMARY OF THE INVENTION

An objective of the invention is to resolve the above-described problem and to provide a method of forming a semiconductor device, which avoid reaching a contact hole to a support substrate of a SOI substrate through a BOX layer.

The objective is achieved by a method of manufacturing a semiconductor

device, including the steps of, (1) preparing an SOI substrate, (2) forming a metal layer on the SOI substrate, (3) performing a first anneal treatment to the metal layer at a relatively low temperature in order to transform the metal layer to a first silicide layer, (4) forming an insulating layer on the first silicide layer, and (5) forming a contact hole, which reaches the first silicide layer, in the insulating layer; and (6) performing a second anneal treatment to the silicide layer at a relatively high temperature in order to transform the first silicide layer to a second silicide layer.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be more particularly described with reference to the accompanying drawings, in which:

Figs. 1A through 1H are sectional views showing successive stages in manufacturing an SOI-type semiconductor device; and

Fig. 2 is a graph showing a BOX yield.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In each drawing, the same reference numbers designate the same or similar components.

Figs. 1A through 1H shows successive stages in manufacturing an SOI-type semiconductor device 100. Referring to Fig. 1A, a buried silicon oxide layer (BOX layer) 20 is formed on an entire surface of a support substrate 10 made of silicon. Then, a silicon-on-insulator layer (SOI layer) 30 is formed on an entire surface of the

BOX layer 20. An SOI substrate consists of the support substrate, the BOX layer and the SOI layer. Then, a cobalt layer (Co layer) 40 having an appropriate thickness is formed on the SOI layer 30 by a conventional sputtering method . After forming the Co layer 40, a titanium nitride layer (TiN layer) 50 is formed on the Co layer 40 by a conventional sputtering method. The TiN layer 50 acts as a cap layer to protect the reaction of the Co layer 40 with the SOI layer from the atmosphere in a successive silicidation process.

Referring to Fig. 1B, a first anneal treatment is performed to the SOI-type semiconductor device 100 in the range between 450 ℃ and 550 ℃, preferably 550 ℃ for thirty (30) seconds whereby a CoSi silicide layer 45 is formed as a result of a reaction of the SOI layer 30 and the Co layer 40. Here, 450 ℃ is the minimum temperature in order to form the CoSi silicide layer 45, and 550 ℃ is the maximum temperature to avoid forming any voids in the silicide layer 45 by using to much silicon in the SOI layer 30. Then, an unreacted part of the Co layer 40 and the TiN layer 50 are removed by a wet etching method.

Referring to Fig. 1C, a plasma SiO_2 layer 60, which as an interlayer oxide film, is, then, formed on the CoSi silicide layer 45 under the condition in the range between 400 ℃ and 550 ℃, preferably 440 ℃. The temperature range for forming the plasma SiO_2 layer 60 is relatively lower than that for forming a LP-TEOS SiO_2 layer, which is generally formed in the atmosphere around 700 ℃. Here, 450 ℃ is the minimum temperature in order to form the plasma SiO_2 layer 60, and 550 ℃ is the

maximum temperature to avoid forming any voids in the silicide layer 45 as described above.

Figs. 1D through 1H shows successive stages in forming an imperceptible mask pattern in order to form a contact hole in the SOI-type semiconductor device 100. With an increase in high integration of a system LSI, a size of the contact hole formed in an interlayer is getting smaller. In the generation that the gate length is 0.1 μm, it is required to form a contact hole having less than 0.1μm at its diameter, which is out of the resolution limit of a KrF photolithography. To satisfy this requirement, a couple of techniques are proposed for mass production purpose. One of these techniques is a method of making a contact hole by SAC (Self Aligned Contact) etching after a hole pattern whose size is resolutionable by photolithography is formed in a resist layer. Another is a method of making a contact hole whose diameter at the bottom is reduced less than 0.1μm by a taper etching method. The other is an introduction of mask shrink processes. Specifically, according to the mask shrink process using poly-silicon (Poly-Si), it is possible to make an imperceptible contact hole less than 0.1μm consistently.

As described above, Figs. 1D through 1H shows successive stages in forming an imperceptible mask pattern in order to form a contact hole patterns in the SOI-type semiconductor device 100. Specifically, the poly-Si mask shrink process is applied to these successive stages. As shown in Fig. 1D, a first poly-Si layer 70, which acts as a mask, is formed on the entire surface of the plasma SiO_2 layer 60. Then, a hole

pattern 75 having a width less than 0.2 μm is formed in the first poly-Si layer 70 by the conventional KrF photolithography and the dry etching technology. Generally, the resolution limit of the KrF photolithography is approximately 0.2μm.

Referring to Fig. 1E, a second poly-Si layer 80 is, then, deposited on the first poly-Si layer 70 and in the hole pattern 75. The thickness of the first poly-Si layer 70 is determined by the depth of the contact hole. Deeper the contact hole is formed, thicker the first poly-Si layer 70 is required. However, when the first poly-Si layer 70 is formed thick too much, the etching for making a contact hole may stop accidentally. Thus, in this embodiment, the thickness of the first poly-Si layer 70 is set at less than 5000 Å, preferably 3000 Å. On the other hand, the thickness of the second poly-Si layer 80 is determined by the width of the contact hole. In this embodiment, since the width of the contact hole is set at 0.1μm, the thickness of the second poly-Si layer 80 is set at 1000 Å.

The first and second poly-Si layers 70, 80 are formed in the same material and under the same condition. Thus, the quality of them are the same. When the quality of the first and second poly-Si layers 70, 80 are the same, these layers can be etched out uniformly.

Then, referring to Fig. 1F, the second poly-Si layer 80 is etched out by an anisotropical etching so that a poly-Si side-wall spacer 85 is formed at the internal surface of the hole pattern 75. According to this method, since the poly-Si side-wall spacer 85 is formed in the hole pattern 75, the size of the actual contact hole 75A is

less than 0.1μm, which is smaller than the resolution limit. According to this step, a poly-Si mask 88 formed by the first poly-Si layer 70 and the poly-Si side-wall spacer 85 is completed.

As described above, the first and the second poly-Si layers 70, 80 are deposited in the range between 400 ℃ and 550 ℃, preferably 540 ℃, which is less than 620 ℃ at which a poly-Si layer is generally formed in this field. Depositing the first and the second poly-Si layers 70, 80 under this condition avoids forming any voids of the CoSi silicide layer 45 while the quality of the first and the second poly-Si layers 70, 80 is maintained.

Next, referring to Fig. 1G, a contact hole 90, which reaches the CoSi silicide layer 45, is formed in the plasma SiO_2 layer 60 by using the poly-Si mask 88. Generally, a poly-Si layer, which is deposited in the atmosphere less than 620 ℃, is in amorphous state. Thus, the resistance of such a poly-Si layer to the dry etching, which is generally used in this field, is not sufficient acting as a mask. For this reason, the dry etching using the amorphous state poly-Si mask 88 for forming the contact hole 90 is performed under the condition below.

Etching device: Dipole ring magnetically enhanced reactive ion etching system

Gas condition: $C_4F_8/O_2/Ar$=20/10/500 sccm, 40mTorr, 1600W or

CHF_3/CO=30/170 sccm, 35mTorr, 1600W

It is confirmed that the amorphous state poly-Si layer deposited in the atmosphere less than 620 ℃ has dry etching resistance enough to form the contact

hole having a width of 0.1μm when the dry etching is performed under the condition described above.

Next, referring to Fig. 1H, after the contact hole 90 is formed, a second anneal treatment, that is a rapid thermal anneal, is performed to the SOI-type semiconductor device 100 in the atmosphere of 800 ℃ for thirty (30) seconds so that the CoSi silicide layer 45 is transformed to $CoSi_2$ silicide layer 48. Generally, the CoSi silicide layer 45 itself shown in Fig. 1B, which is formed in the atmosphere of 550 ℃, is not suitable for applying it to a semiconductor device because of its high specific resistance. For this reason, it is necessary to perform the second anneal treatment, as shown in Fig. 1H.

According to the invention, this second anneal treatment is performed after the contact hole 90 is formed, as described above. On the other hand, as described in the description of the related art, the second anneal treatment is performed just after the first anneal treatment. When the second anneal treatment is performed just after the first anneal treatment, some voids are formed in the $CoSi_2$ layer because silicon in the SOI layer 30 is further consumed by reaction for transforming to $CoSi_2$ from CoSi. Thus, the contact hole 90 may reaches to the BOX layer 20 when the contact hole 90 is formed in the plasma SiO_2 layer 60 on an area where the void is formed in the $CoSi_2$ layer 48. Since the plasma SiO_2 layer 60 is formed of the same material of the BOX layer 20, the contact hole 90 may reaches to the support substrate 10 by accidental over-etching. However, according to the invention, since the second anneal

treatment is performed after the contact hole 90 is formed, there is no voids formed in the CoSi layer 45 wherever the contact hole 90 is formed. Thus, it is possible to avoid reaching the contact hole 90 to the BOX layer 20 when the contact hole 90 is formed. After the second anneal treatment, some voids may be formed in the $CoSi_2$ layer 48. However, since the contact hole 90 has been formed at this stage, the contact hole 90 does not contact to the support substrate 10.

Fig. 2 shows experiment results regarding a BOX yield of the thin film SOI-type semiconductor device. In Fig. 2, the thin film SOI-type semiconductor device manufactured by the process described above and the thin film SOI-type semiconductor device manufactured by the process of the related arts are compared. Further, by changing the thickness of the SOI layer of both semiconductor devices, a BOX yield of both semiconductor devices can be compared. As shown in Fig. 2, in the case that the thickness of the SOI layer is formed at 20nm, a BOX yield can be 100%, which means no defectives, in the device formed by the invention. On the other hand, a BOX yield is 0%, which means all defectives, in the device formed by the related art.

According to the invention, since all process steps before forming the contact hole 90 are performed under 550 ℃, it is possible to avoid forming voids in the silicide layer. Thus, it is possible to increase the BOX yield dramatically. Further, since the second anneal for transforming the CoSi layer 45 to the $CoSi_2$ layer 48 is performed after the contact hole 90 is formed, there is no voids formed in the CoSi layer 45 when the contact hole 90 is formed. Thus, the contact hole does not reach to the BOX

layer 20. As the result, it is possible to reduce the BOX defects when the contact hole 90 is formed.

While the invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various other modifications of the illustrated embodiment will be apparent to those skilled in the art on reference to this description. Therefore, the appended claims are intended to cover any such modifications or embodiments as fall within the true scope of the invention.